

Title: A High Speed Memory Interface System and Method

Docket #: CYPR-CD01080

Inventor(s): Gabriel Li

Serial #: 10/032,248

Filing Date: 12/21/01

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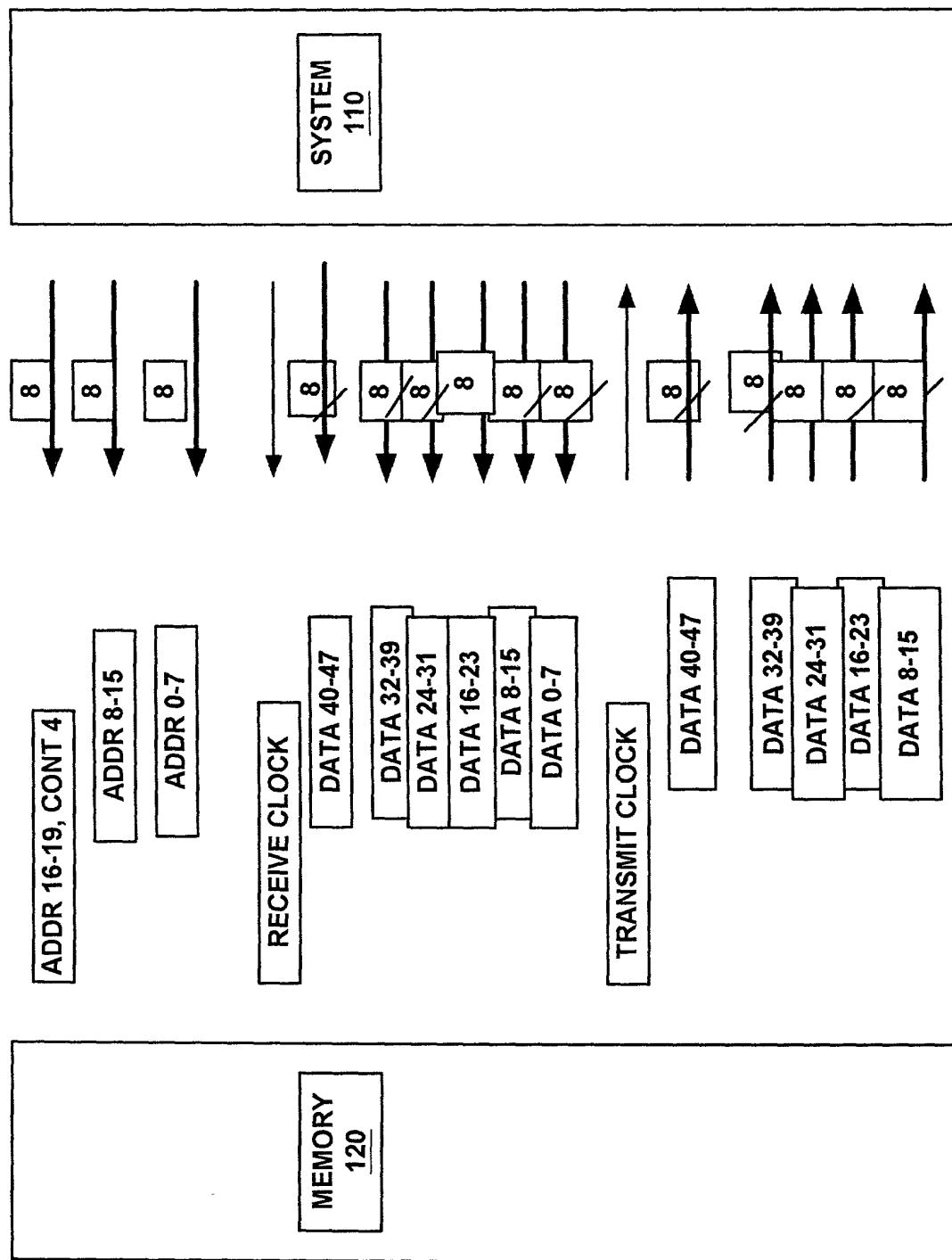


FIGURE 1

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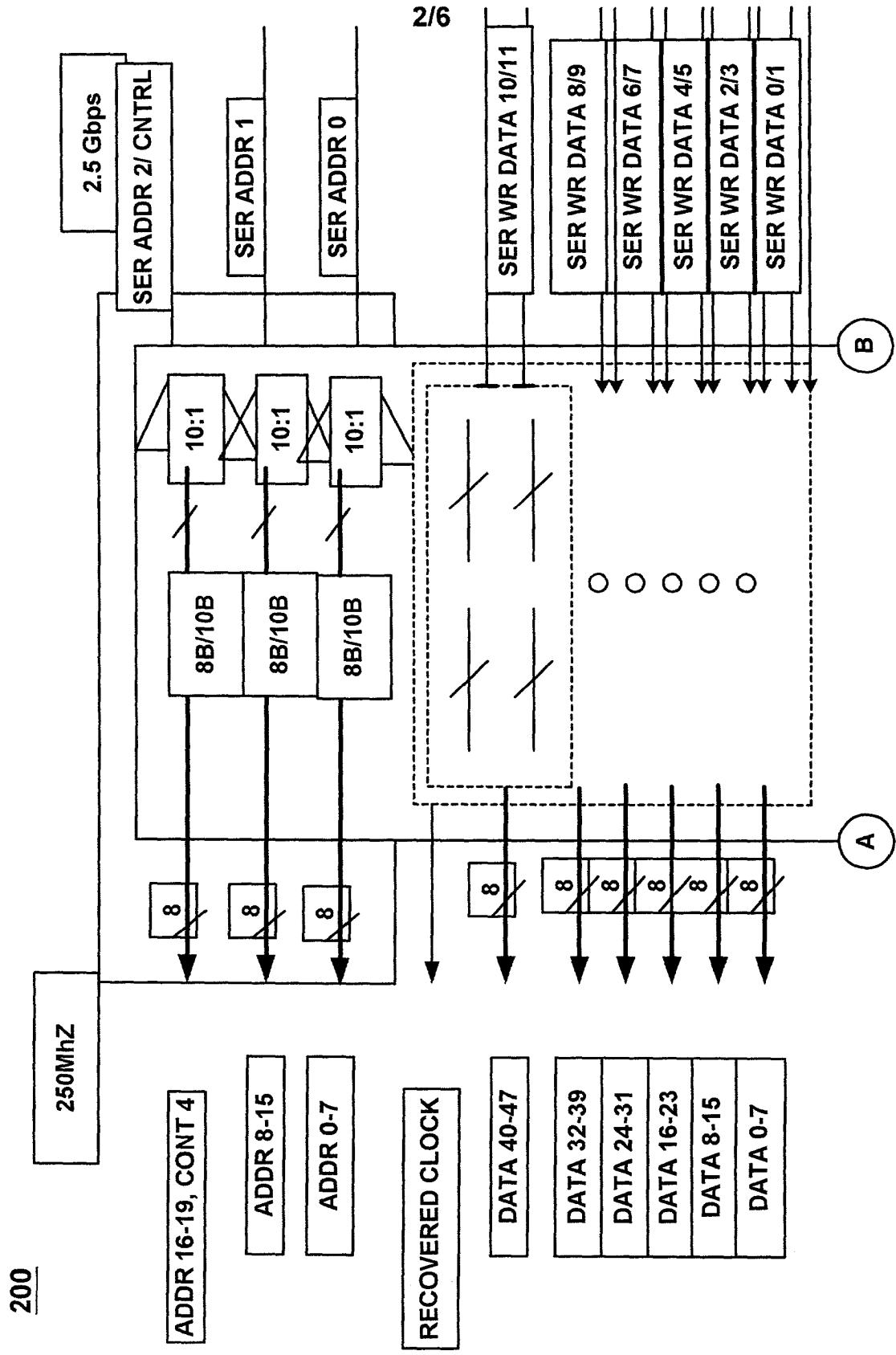
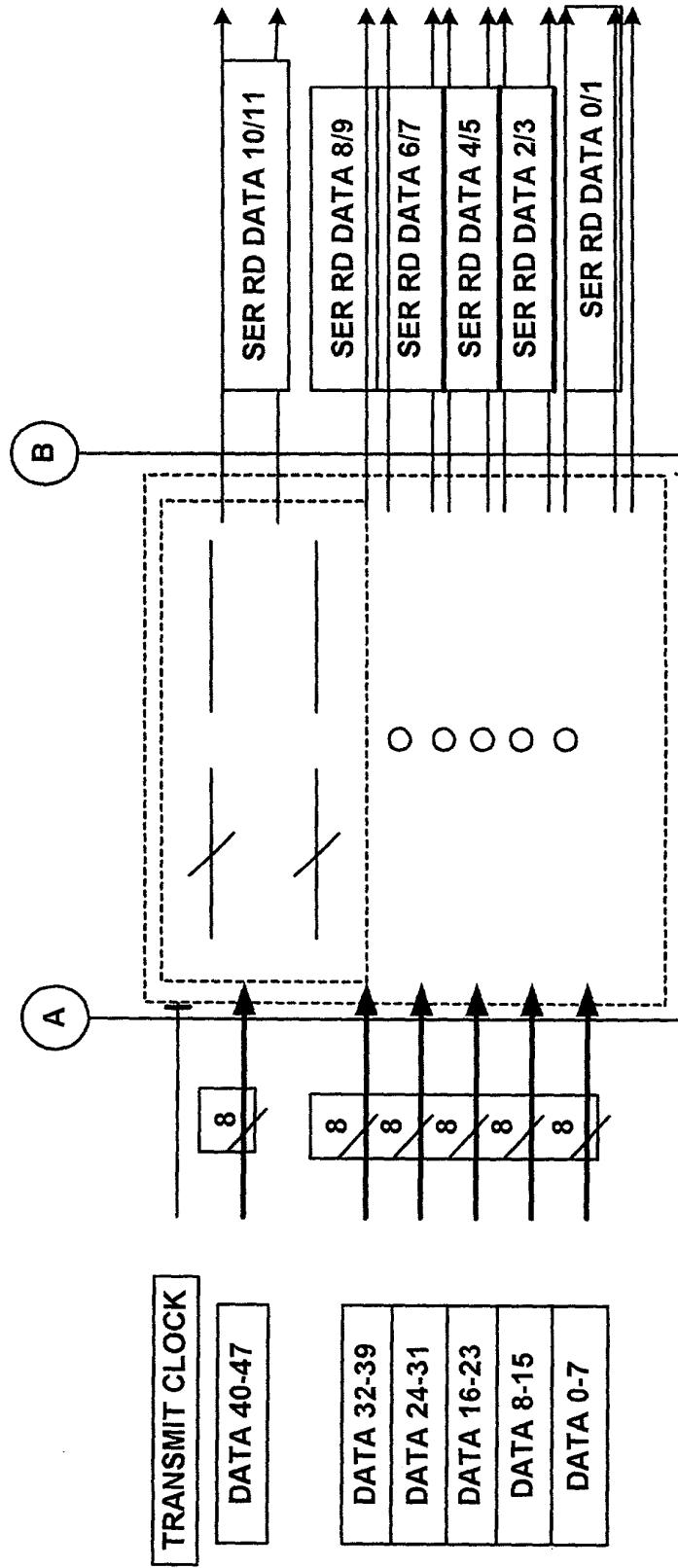


FIGURE 2

200 (CONT.)



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**FIGURE 2 (CONT.)**

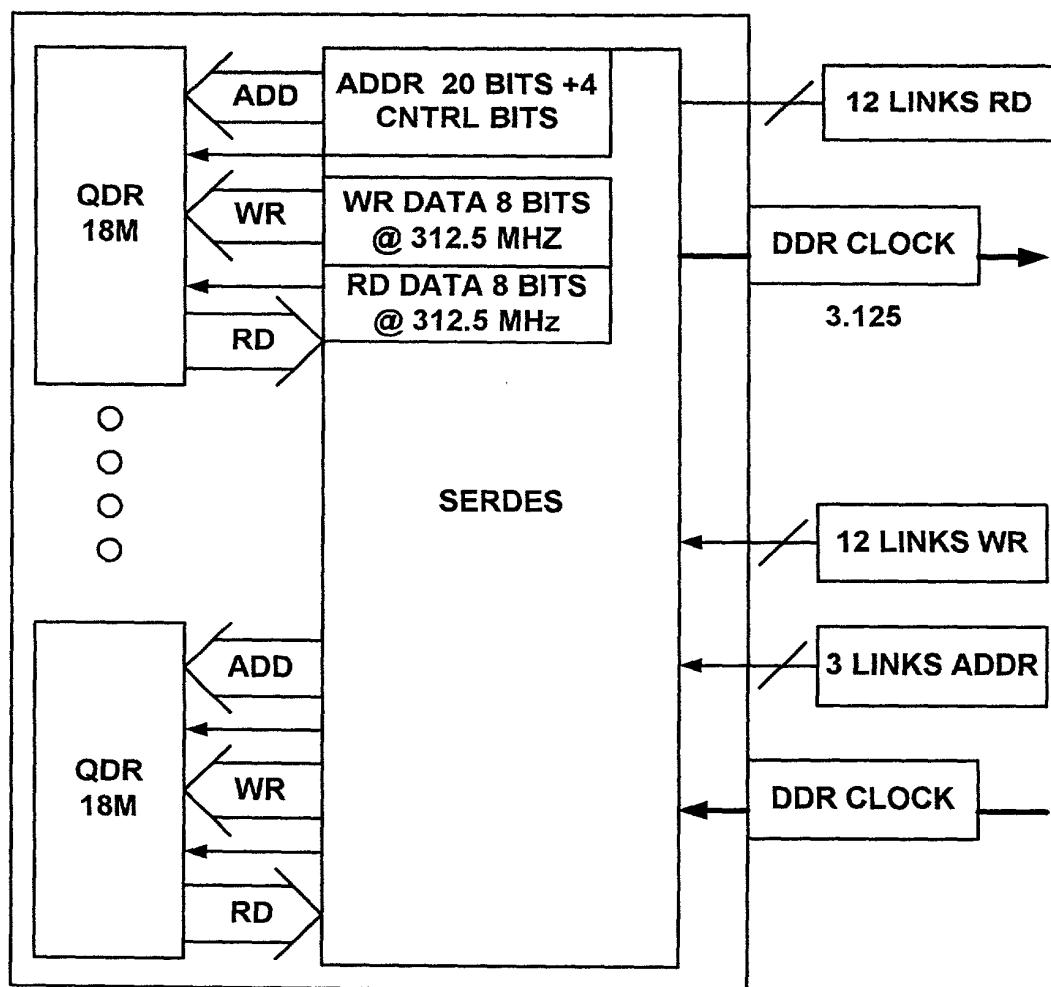


FIGURE 3

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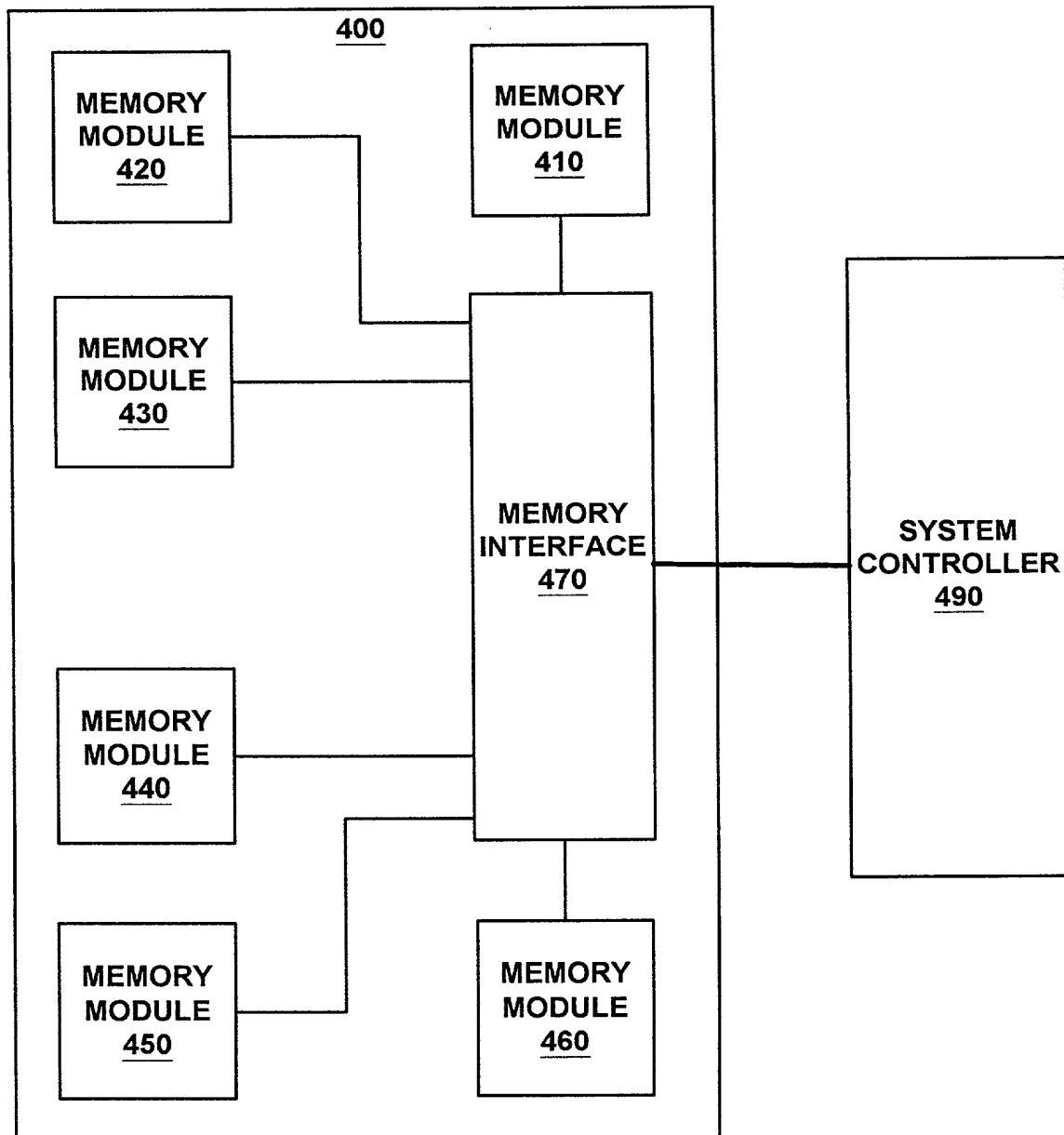
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**FIGURE 4**

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**ENGAGING IN SERIAL COMMUNICATIONS AT A FIRST RATE  
WITH A SYSTEM MEMORY CONTROLLER.**

510

**EXECUTING PARALLEL COMMUNICATIONS WITH A MEMORY  
ARRAY AT A SECOND RATE.**

520

**CONFIGURING THE INFORMATION IN PROPER ALIGNMENT  
FOR COMMUNICATION BETWEEN SERIAL SYSTEM  
CONTROLLER SIGNALS AND PARALLEL MEMORY ARRAY  
SIGNALS.**

530

**FIGURE 5**